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And Rd Rn Rm Op

Cond 0 0 0 0 0 0 A S Rd Rn Rs 1 0 0 1 Rm Multiply Cond 0 0 0 0 1 U A S RdHi RdLo Rn 1 0 0 1 Rm Multiply Long ... cRn := rRn {<op>cRm} 4.16 MLA Multiply Accumulate Rd := (Rm * Rs) + Rn 4.7, 4.8 MOV Move register or constant Rd : = Op2 4.5 MRC Move from coprocessor register to CPU register Rn := cRn {<op>cRm} 4.16

4 ARM Instruction Set - GitHub Pages

We can also specify a flexible second operand in the form Rm {,shift}. If Rd is missing, Rn is also the destination. For example: ADD Rd, Rn, Rm {,shift} ;Rd = Rn+Rm ADD Rn, Rm {,shift} ;Rn = Rn+Rm. where Rm is the register holding the data for the second operand, and shift is an optional

shift to be applied to Rm.

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